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Inventor(s): Hiroshi Takahara

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SPECIFICATION

1. Title of the Invention

Liquid Crystal Display Panel and Manufacturing Method Therefor

2. Claim

(1) A liquid crystal display panel, wherein a switching element for driving a picture element and a scanning circuit for applying a signal to a gate signal line to which said switching element is connected are formed on a semiconductor substrate, and a driving IC is connected to a source signal line to which said switching element is connected through a conductive junction layer.

(2) The liquid crystal display panel as claimed in claim 1, wherein an output current control circuit is formed on an output part of a scanning circuit.

(3) The liquid crystal display panel as claimed in claim 1, wherein a plurality of switching elements are formed on one picture element.

(4) The liquid crystal display panel as claimed in claim 1, wherein an inspection electrode is formed between an electrode to which a driving IC is connected and a display region where a switching element is formed.

(5) The liquid crystal display panel as claimed in claim (2), wherein said output current control circuit is adapted to switch between the normal output current state and the output current limiting state according to an applied signal of an external input signal.

(6) A method for manufacturing a liquid crystal display panel,

comprising the steps of: forming a switching element for driving a picture element and a scanning circuit on a polysilicon substrate; installing a substrate where a counter electrode is formed on said substrate; injecting liquid crystal between said substrates to be formed into a panel; operating said scanning circuit; conducting an inspection process for said liquid crystal panel by use of an inspection pad; and subsequently connecting a driving IC where a projecting electrode is formed to a source signal line through a conductive junction layer.

(7) The method for manufacturing a liquid crystal panel as claimed in claim (6), wherein said inspection process is conducted by detecting an electric current flowing through a source signal.

3. Detailed Description of the Invention

Field of the invention

This invention relates to a liquid crystal display panel used in an active matrix type liquid Crystal device and a manufacturing method therefor.

Prior art

Recently with the increase in the number of picture elements of a liquid crystal display device, the number of scanning lines has been increased, and in the conventional simple matrix type liquid crystal display device, the display contrast and the response speed are deteriorated, so an active matrix type liquid crystal display device having a switching element in each picture element has been utilized. However, it is necessary to form tens of thousands or more of thin film transistors (hereinafter referred to as TFT) in an active matrix array used in the above liquid crystal display device. Accordingly, it is difficult to manufacture all active matrix arrays without defect, and in the present technology, it is necessary to inspect the TFT formed on the active matrix array to discriminate the quality. So the liquid crystal display panel in which the TFT on the active matrix array can be easily inspected and a manufacturing method therefor have been expected.

The conventional liquid crystal display panel will now be described with reference to the attached drawings. Figure 9(a) is a

plan view of the conventional liquid crystal display panel. Figure 9 (b) is a cross sectional view taken along line EE' of Figure 9 (a). Parts not needed for description are omitted, and to facilitate the description, enlarged or exaggerated parts are existent. Further in order to facilitate drawing figures, the number of signal lines and the number of IC of the liquid crystal panel are considerably reduced. So with the following drawings.

In Figures 9 (a) and (b), 90 is a liquid crystal, 91 is a substrate formed by soda glass, 92 is a substrate where a counter electrode is formed (hereinafter referred to as a counter substrate), 93 is a gate signal line, 94 is a source signal line, 95 is a connecting electrode forming part formed on the substrate 91 for connection to a flexible substrate 96, the reference numeral 96 is a flexible substrate for connecting a gate or source signal line and a lead wire 101 on the substrate 97 loaded with IC, 97 is a printed wiring board to be loaded with a scanning IC 98 or a source IC 99 (hereinafter referred to as IC substrate), 98 is an IC for applying a signal to the gate signal line 93 of the liquid crystal display panel (hereinafter referred to as scanning IC), 99 is an IC for applying a signal to the source signal line 94 of the liquid crystal display panel (hereinafter referred to as source IC), and 100 is resin for sealing a liquid crystal 90 between the substrate 91 and the counter substrate 92 (hereinafter referred to as sealing resin). Hereinafter the same reference numbers and the same symbols designate the same constitution or the same content. Figure 10 is a partial equivalent circuit diagram of a TFT group formed on a part on the substrate 91, which faces to the liquid crystal. In Figure 10, $T_{11} \sim T_{44}$ are TFT, $S_1 \sim S_4$ are source signal lines, $G_1 \sim G_4$ are gate signal lines, and $P_{11} \sim P_{44}$ are picture element electrodes. Figure 11 is a partial enlarged plan view of the connecting electrode forming part 95. In Figure 11, the reference numeral 110 is a connecting electrode.

As is clear in Figures 9 11, in the conventional liquid crystal panel, a TFT group and a connecting electrode are formed on the glass substrate 91 and further a counter substrate is installed to be formed into a panel. The IC for applying a signal to the said panel

is loaded on the IC substrate 97 by soldering, and the substrate and the panel are connected to each other by the flexible substrate 96. An anisotropic conductive film is used for connecting the flexible substrate 96, and the flexible substrate 96 and the connecting electrode, and the flexible substrate 96 and the lead wire 101 are connected to each other by hot thermocompression bonding.

A manufacturing method for the conventional liquid crystal display panel will now be described. Figure 12 (a) is a plan view of a substrate after an array forming process. Figure 12 (b) is a cross sectional view taken along line FF' of Figure 12 (a). In Figures 12 (a) and (b), 120 is a TFT group forming part shown in Figure 10 (hereinafter referred to as display region). First, in the array forming process, a metal thin film and an amorphous silicon thin film or the like are stacked in layer on soda glass, and a display region 120, signal lines 93,94 and a connecting electrode 110 are formed. Figure 13 (a) is a plan view of a substrate after a panelling process. Figure 13 (b) is a cross sectional view taken along line G G' of Figure 13 (a). After the array forming process, the substrate is sent to the panelling process. In this process, a counter substrate 92 is installed on the display region, and the peripheral part is sealed with sealing resin, and to a liquid crystal 90 is injected. After the end of the process, a non-defective unit is sent to the next inspection process. Figure 14 is a diagram for explaining the inspection process. In Figure 14, the reference numeral 140 is a short generated at the intersectional point of a gate signal line G3 and a source signal line S3 (hereinafter referred to as cross short), 141 is resistance value measuring means, $PS_1 \sim PS_4$ and $PG1 \sim PG_4$ are connecting means such as a probe or the like (hereinafter referred to as probe). $SS_1 \sim SS_4$ and $SG_1 \sim SG_4$ are select means comprising a relay or an analog switch or the like (hereinafter referred to as switch). In the inspection process, it is an object to mainly detect cross short which becomes a critical display defect. In this process, the probes $PG_1 \sim PG_4$ are pressed to the gate signal lines $G_1 \sim G_4$ of the liquid crystal display panel, and the probes $PS_1 \sim PS_4$ are pressed to the source signal lines. Normally 200 or more

signal lines of the liquid crystal display panel are formed, so it is difficult to press the probes to all signal lines at one time. Then, the probes are installed on an XY stage or the like and moved to be sequentially pressed, and inspection is performed. After pressing the probes, only the switch SS_1 is closed and the switches SG_1 to SG_4 are sequentially closed to measure the resistance value in each state by the resistance value measuring means 141. In order to conduct the above operation for all gate signal lines, the probes $PG_1 \sim PG_4$ are sequentially moved to conduct the operation. Subsequently, only the switch SS_2 is closed, and similarly the switches SG_1 to SG_4 are sequentially closed. On the other hand, the probes $PG_1 \sim PG_4$ are moved to conduct the operation. By performing the above operation with the switches $SS_1 \sim SS_4$ sequentially closed and moved, the resistance value between all gate signal lines and the source signal lines are measured. The resistance value is measured as high resistance if the intersectional point of the gate signal line and the source signal line is normal, and if short-circuited, low resistance is measured. In Figure 14, since cross short 140 is caused, when the switches SG_3 and SS_3 are closed, a low resistance value is measured. The unit in which cross short is caused is discarded as defective unit. The connecting process will now be described. In the connecting process, first the scanning IC 98 or the source IC 99 is loaded on the IC substrate 97. Subsequently, an anisotropic conductive film is formed on the flexible substrate 96. Next, the flexible substrate 96 is positioned according to the position of the lead wire 101 of the IC substrate 97 and the connecting electrode forming part 95 and then connected to each other by thermocompression bonding. A liquid crystal display panel is completed through the above processes.

Problems to be solved by the invention

Nowadays the space of signal lines of the liquid crystal display panel has a tendency to be made fine to 200 μm or less. Further, the number of signal lines has a tendency to increase to hundreds or more. Accordingly, in the conventional liquid crystal display panel and manufacturing method therefor, the following serious

problems are caused in the inspection process. In the liquid crystal display panel, it is necessary to detect cross short which becomes a critical display defect in the inspection process to discriminate the quality of the liquid crystal display panel. Further it is preferable to detect a source-drain open circuit of the TFT which becomes a black spot-like display defect (hereinafter referred to as S.D open), gate-drain short (hereinafter referred to as G.D short), and a source-drain short of the TFT which becomes a white-spot like display defect (hereinafter referred to as S.D short). In order to perform the described inspection, it is necessary to press the probe to a source signal line of the liquid crystal display panel and a draw-out electrode of a gate signal line to make electric connection. However, the draw-out electrode of the signal line has a tendency to be made fine, so it becomes gradually difficult to position the probe accurately. The more the microprocessing is advanced, the longer positioning time is required. The number of signal lines of the liquid crystal display panel also has a tendency to be increased, and as the number of probes to be pressed at one time is limited, the number of times of moving the probe is increased and long time is needed for the inspection. For example, even if the number of signal lines is 200 x 400, when 25 x 25 probes are pressed at one time and 25 x 25 probes are inspected each for 10 seconds, about 20 minutes are needed for the inspection. Further, point defects such as S.D short, G.D short and S.D open defects can be hardly detected in the conventional inspection process, and ordinarily the detection is not performed. Concerning the described point defects, after the liquid crystal display panel is perfectly completed, inspection by display is performed to discriminate the quality. However, when defective units are found after completion, the rate of rebounding to the manufacturing cost is large, and it is a serious problem.

Means for solving the problems

In order to solve the above problems, according to the present invention, a liquid crystal display panel comprises a switching element for driving a picture element and a scanning circuit for applying a signal to a gate signal line to which the switching

element is connected, formed to a polysilicon substrate, and a driving IC where a projecting electrode is formed is connected to a source signal line to which the switching element is connected through a conductive junction layer.

Further, a method for manufacturing a liquid crystal display panel of the present invention comprises the steps of: forming a switching element for driving a picture element and a scanning circuit to a polysilicon substrate; installing a substrate where a counter electrode is formed on the said substrate; injecting liquid crystal between the said substrates to be formed into a panel; operating the scanning circuit; conducting an inspection process for the liquid crystal panel by use of an inspection pad; and subsequently connecting a driving IC where a projecting electrode is formed to a source signal line through a conductive junction layer.

Operation

The liquid crystal display panel of the present invention is provided with a TFT for driving a picture and a scanning circuit formed to a polysilicon substrate. By operating the scanning circuit, voltage for operating the TFT (hereinafter referred to as ON- state voltage) or voltage for not operating the TFT (hereinafter referred to as OFF-state voltage) can be applied to an arbitrary gate signal line. Accordingly, the probes are pressed to all gate signal lines at one time to obtain the similar effect to that in the case of applying a signal. Further, according to the method for manufacturing the liquid crystal display panel of the present invention, as the source IC is loaded after the inspection on the liquid crystal display panel, it is not necessary to consider the input impedance of the source IC at the time of inspection. Accordingly, sure and stable inspection can be performed.

Embodiment

One embodiment of a liquid crystal display panel according to the present invention will now be described with reference to the attached drawings. Figure 1 (a) is a plan view of a liquid crystal display panel according to the present invention. Figure 1 (b) is a cross sectional view taken along line AA' of Figure 1 (a), and Figure

1 (c) is a cross sectional view taken along line B B' of Figure 1 (a). In Figures 1 (a), (b), (c), 10 is a liquid crystal, 11 is a semiconductor substrate consisted of polysilicon or the like, 12 is a counter substrate, 13 is a part where an electrode for inspecting the liquid crystal display panel is formed (hereinafter referred to as an inspecting electrode forming part), 14 is a chip-like source IC, 15 is a gate signal line, 16 is a source signal line, 17, 18 are lead wires, 19 is a forming part of a scanning circuit for applying and scanning ON-state voltage or OFF-state voltage to a gate signal line, and 20 is sealing resin. As is clear in Figures 1 (a), (b) and (c), the liquid crystal display panel of the present invention is provided with a TFT and a scanning circuit formed to a polysilicon substrate. Further in the periphery of a display region, an inspection electrode corresponding to each signal line is formed, and a source IC 14 chip is connected to the source signal line by glass on chip technology (hereinafter referred to as COG technology). Further the liquid crystal display panel of the present invention will be described with reference to Figures 2 $\sim$ 4. First, Figure 2 is a partial equivalent circuit diagram of a display region part where a TFT is formed. In Figure 2, $TM_{11} \sim TM_{24}$ and $TS_{11} \sim TS_{44}$ are TFT. As is clear in Figure 2, in the liquid crystal display panel of the present invention, two TFTs are formed on one picture element electrode and the above two TFTs are respectively connected to different gate signal line and source signal line. Figure 3 (a) is a partial enlarged plan view of a source IC 14 and lead wire 18 part. In Figure 3 (a), 30 is an electrode formed on the substrate 11 for connection to the terminal of the source IC 14 chip (hereinafter referred to as IC connecting electrode), and a dotted line indicated by 31 shows the loading position of the source IC 14 chip. As described above, the source IC 14 chip is connected to the source signal line of the liquid crystal display panel of the present invention through the IC connecting electrode 30. Figure 3 (b) is a block diagram of a scanning circuit of a scanning circuit forming part 19. In Figure 3 (b), 32 is a shift register circuit, 33 is a latch circuit for latching and retaining the logical output of the shift

register circuit 32, 34 is a drive circuit for outputting ON-state voltage and OFF-state voltage according to the logical output of the latch circuit 33, and 35 is an output current limiting circuit having a function of limiting the current input and output to and from the output terminals $X_1 \sim X_n$ to a regulated value or less. The output current limiting circuit 35 is capable of releasing or operating a limiting function of an input/output current according to the logical input of the CL terminal. Normally during the inspection process, it is operated, and in the display state, it is released. The shift register circuit 32 outputs the logical output with H or L level according to data which a clock Ø is inputted to SP^1 or SP^2. The above logical output is passed through the latch circuit 33 or retained in the latch circuit 33, and ON-state voltage or OFF-state voltage are outputted from the drive circuit. Figure 4 is a partial enlarged plan view of an inspection electrode forming part 13. In Figure 4, the reference numeral 41 is an inspection electrode. As is clear in Figure 4, all source signal lines or gate signal lines are drawn out to the inspection electrode 41. From the inspection electrode 41, they are drawn out one by one to be guided to the scanning circuit forming part 19 or the IC connecting electrode 30. The above inspection electrode 41 is formed at least in the source signal line.

The method for manufacturing a liquid crystal display panel of the present invention will now be described. Figure 5 (a) is a plan view of the substrate 11 after the array forming process. Figure 5 (b) is a cross sectional view taken along line CC' of Figure 5(a). First, in the array forming process, a TFT, a scanning circuit and so on is formed to a polysilicon substrate by semiconductor technology. Further, an IC connecting electrode 30 is formed, too. After the array forming process, it proceeds to the next panelling process. Figure 6 (a) is a plan view of a substrate after the panelling process. Figure 6 (b) is a cross sectional view taken along line DD' of Figure 6 (A). In this process, a counter substrate 12 is installed on a display region where the TFT is formed, and after the peripheral part is sealed with sealing resin, the space between the

said substrates is evacuated and a liquid crystal 10 is injected. After the end of the above process, a non-defective unit advances to the next inspection process. Figure 7 is a diagram for explaining a liquid crystal display panel in the inspection process. In Figure 7, in order to facilitate description, a scanning circuit 19 is drawn only on the left side of the drawing. In Figure 7, the reference 70 is S.D short , 71 is G.D short, 74 is cross short, 72 is signal applying means for applying d.c. voltage, 73 is signal detecting means for detecting signals, for example, a current or the like, QS_2, QS_4 are probes, and US_2, US_4 are switches. First, the detection method for cross short 74 will be described. The probes $PS_1 \sim PS_5$ are pressed to the inspection electrode 41 formed on the end of the source signal line. Subsequently, the scanning circuit 19 is operated to apply OFF-state voltage to all gate signal lines. Here, OFF-state voltage is taken as - voltage, and ON-state voltage is taken as + voltage. Next, the switches SS_1 to SS_5 are sequentially closed one by one, and in each state, the presence/absence of output voltage or current is measured by signal detecting means 73. As cross short 74 occurs now, when the switch SS_3 is closed, OFF-state voltage is detected by the signal detecting means 73. Accordingly, it is known that the source signal line S_3 and the gate signal line are short-circuited. Subsequently, with the switch SS_3 closed, ON-state voltage is applied to the gate signal line G_1 and sequentially shifted to the last gate signal line. In the above described respective states, whether there is the change in the OFF-state voltage or not is monitored by the signal detecting means 73. When ON-state voltage is applied to the gate signal line G_3, a signal detected by the signal detecting means 73 changes from OFF-state voltage to ON-state voltage. Accordingly, the occurrence of cross short in the gate signal line G_3 and the source signal S_3 can be detected. Since the output current limiting circuit 35 is formed in the scanning circuit 19, even if cross short occurs, or even if adjacent short of the gate signal line occurs, overcurrent will not flow, and that is why the panel and the scanning circuit can be stably inspected without breakage.

The inspection can be performed by conducting the above

operation to the other source signal lines by moving the probes $PS_1 \sim PS_5$.

The detecting method for C.D short 71 will now be described. First the probes $PS_1 \sim PS_5$ are pressed to the inspection electrode 41 formed on end of the source signal line. Next, the scanning circuit 19 is operated to apply ON-state voltage to the gate signal line G_1 and apply OFF-state voltage to the other gate signal lines. At that time, select means, SS_1 to SS_5, are closed sequentially and selectively, and the presence/absence of output current in each source signal line is measured by the signal detecting means 73. The above operation is conducted for all of the gate signal lines similarly to the description on the cross short. When ON-state voltage is applied to the gate signal line G_4 and the select means SS_3 is closed, G.D short 71 occurs in TM_{33} of the TFT and the TM_{33} of the TFT is in the operating state, so that a current path, the gate signal line G_4 -> G.D short 71 -> TM_{33} drain -> TM_{33} source -> source signal line S_3 -> PS_3 -> SS_3 -> the signal detecting means 73, is produced, from which the occurrence of defect in the TM_{33} of the TFT can be detected. The above operation is conducted for all source signal lines by moving the probes.

Lastly the detection method for S.D short will be described. First, the probes $PS_1 \sim PS_5$ and QS_2, QS_4 are pressed to the inspection electrode 41. Subsequently, the scanning circuit 19 is operated to apply ON-state voltage only to the gate signal line G_1 and apply OFF-state voltage to the other gate signal lines. Next, the select means US_2 and US_4 are closed to apply voltage from the signal applying means 72 to the souse signal lines S_2 and S_4. Subsequently, the select means SS_1, SS_3, SS_5 are closed sequentially and selectively to measure the presence/absence of output voltage in the respective source signal lines S_1, S_3, S_5 by the signal detecting means 73. Next, ON-state voltage is applied only to the gate signal line G_3 and the above operation is conducted. The above operation is performed for all of the gate signal lines. As S.D short 70 occurs in the TM_{22} of the TFT, ON-state voltage is applied to the

gage signal line G2, and the TS22 of TFT is put in the operating condition, and when the select means SS_{22} is closed, a current path, the signal applying means 72 -> US_2 -> QS_2 -> source signal line S_2 -> S.D short 70 -> P_{22} -> TS_{22} of TFT -> source signal line S_3 -> PS_3 -> SS_3 -> the signal detecting means 73, is produced, from which the occurrence of S.D short 70 can be detected. The above operation is performed for all of source signal lines by moving the probes.

After the end of the inspection process, a non-defective unit is subjected to the source IC connecting process. Figure 8 is a cross sectional diagram in which the source IC 14 is adhered to the IC connecting electrode 30. In Figure 8, the reference numeral 80 is a projecting electrode, and 81 is a conductive junction layer. The above projecting electrode is consisted of An and formed on the terminal of the source IC 14 like a two-stage projection by use of ball bonding or nail head bonding technology. Further a conductive junction layer several tens of μm thick is formed on the above projecting electrode. The conductive junction layer is consisted of mixture of epoxy series and phenol series as an adhesive as main agent and flakes of As, Au, Ni, C, Sn, O_2, and formed by transfer or the other technology. The source IC 14 is connected to the IC connecting electrode 41 in respect of electrode through the projecting electrode and the conductive junction layer. Next, the conductive junction layer is final-hardened by means such as an electric oven, a heat column or the like to complete a liquid crystal display panel.

Though in the description of the manufacturing method for the liquid crystal display panel of the present invention, an inspection process is conducted after a panelling process, it is apparent that even if the panelling process is conducted after the inspection process, the same effect can be produced. Accordingly, after the inspection process, the panelling process may be conducted.

Though the liquid crystal display panel of the present invention has two TFTs formed on one picture element electrode, this is not restrictive.

Advantages of the invention

According to the present invention, a liquid crystal display panel is so constructed that a TFT for driving a picture element and a scanning circuit are formed to a semiconductor substrate and a source IC is loaded by COG technology. As the scanning circuit has a comparatively small circuit scale and can be easily formed, the rate of occurrence of defect and failure is low. If the function of the source IC is incorporated in the semiconductor substrate, the circuit for realizing the above function is large so that the defect and failure are liable to occur. Accordingly, the yield of manufacturing the liquid crystal display panel of the present invention is remarkably high as compared with that in which the function of the source IC is incorporated in the semiconductor substrate. Though the liquid crystal display panel connected to the scanning IC by use of the conventional flexible substrate can not cope with the signal line pitch of a fine pattern 100 μm or less, the liquid crystal display panel of the present invention can satisfactorily cope with the above pitch.

In the method for manufacturing a liquid crystal display panel according to the present invention, an inspection process is conducted before the connection of the source IC. In the inspection process, a current generated at the time of S.D short is normally very small, 1 μA or less. Accordingly, if the source IC is put in the connecting state or formed in the inspection process, the input impedance of the above IC influences. So, it is difficult to detect a very small current, so that defect can not be detected. Furthermore, only by operating the scanning circuit, ON-state voltage or OFF-state voltage can be applied to all of gate signal lines at one time. Accordingly, the same effect as that in the case of pressing the probes to all gate signal lines can be produced, and the inspection time is remarkably reduced. Further, it is sufficient to perform pressing of the probes only on the source signal line side, which results in reducing the manufacturing cost of the probes. The liquid crystal display panel of the present invention is so constructed that two TFTs are formed on one picture element electrode and voltage can be applied to all of gate signal lines at one time by a scanning circuit, whereby even S. D open and S. D short

which could not be detected in the conventional liquid crystal display panel can be detected. Thus, after the formation of a scanning circuit, the quality of the liquid crystal display panel can be determined at high speed and easily, so it is very advantageous.

4. Brief Description of the Drawings

Figures 1 (a) ~ (c) are a plan view and cross sectional views of a liquid crystal display panel according to the present invention;

Figure 2 is a partial equivalent circuit diagram of a display region of the liquid crystal display panel according to the present invention;

Figure 3 (a) is a partial enlarged plan view of a source IC connecting part;

Figure 3 (b) is a functional block diagram of a scanning circuit;

Figure 4 is a partial enlarged plan view of an inspection electrode forming part of the liquid crystal display panel according to the present invention;

Figures 5 (a) and (b) ~ Figure 8 are diagrams for explaining a method for manufacturing a liquid crystal display panel according to the present invention;

Figures 9 (a) and (b) are a plan view and cross sectional views of the conventional liquid crystal display panel;

Figure 10 is a partial equivalent circuit diagram of a display region of the conventional liquid crystal display panel;

Figure 11 is a partial enlarged plan view of a connecting electrode forming part for connecting a flexible substrate; and

Figures 12 (a) and (b) ~ Figure 14 are diagrams for explaining the conventional method for manufacturing a liquid crystal display panel.

10, 90: liquid crystal 11, 91: substrate 12, 92: counter electrode 13: inspection electrode forming part 14: source IC 15, 93: , $G_1 \sim C_4$: gate signal line 16, 94, $S_1 \sim S_5$: source signal line 17, 18: lead wire 19: scanning circuit forming part 20, 100: sealing resin $P_{11} \sim P_{44}$: picture element electrode $T_{11} \sim T_{44}$, $TM_{11} \sim TM_{24}$, $TS_{11} \sim TS_{44}$: TFT, 30: IC connecting electrode 31: IC loading

position 32: shift register circuit 33: latch circuit 34: drive circuit 35: output current limiting circuit 41: inspection electrode 70: S.D short 71: G.D short 72: signal applying means 73: signal detecting means 74, 140: cross short $PS_1 \sim PS_4$, $PG_1 \sim PG_4$, QS_2, QS_4: connecting means $SS_1 \sim SS_4$, $SG_1 \sim SG_4$, US_2, US_4: select means 80: projecting electrode 81: conductive junction layer 95: connecting electrode forming part 96: flexible substrate 97: IC substrate 98: scanning IC 99: source IC 101: lead wire 110: connecting electrode 141: resistance value measuring means